SPECTRAL ELECTRONICS

Subject of review

RISK ASSESSMENT — SAMPLE REPORT

Risk Assessment

EMC & Safety pre-compliance review — Open-source PV micro-inverter (OwnTech Foundation)

PROJECT

OwnTech Foundation Micro-Inverter

Prepared for: Owntech

Prepared by: Ignacio de Mendizabal, Spectral Electronics

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01 · Executive summary

Executive summary

We reviewed the OwnTech Foundation open-source PV micro-inverter, intended to convert DC power from a photovoltaic source into AC power suitable for grid-connected applications. The design includes high-voltage DC, power conversion stages, grid-facing AC circuitry, control electronics and protection functions. These characteristics make EMC and safety considerations critical from the early design stage. The certification path targets the EU regime: LVD (IEC 62109-1/-2), EMC (IEC 61000-6-x), grid code (EN 50549) and RoHS.

Overall risk

Medium · 2 high-priority and 4 medium-priority findings across schematic, PCB and safety. The PCB items (copper under the common-mode choke and missing stitching vias) and the isolation high-pot duration are the highest-impact items to close before a formal lab campaign.

Top findings (preview)

- [R-EMC-P-01] Copper pour of DGND under the common-mode choke FL3 creates high-frequency coupling that reduces or cancels its effectiveness — high risk for conducted EMC.
- [R-EMC-P-02] Solid ground planes on the 4-layer stack-up have long return paths and few stitching vias, causing ground bouncing, common-mode noise and EMC margin loss.
- [Safety-01] Common-mode choke FL3 (PDMCAT18107-102MLB) is hi-pot tested for 3 s, while IEC 62109 demands 60 s after humidity preconditioning — the part may not meet the standard.
- [Safety-02] Four 4.7 nF Y-capacitors to PE may push leakage current near the 3.5 mA AC safety limit; capacitance and parasitics need to be re-checked.

Recommendation

Close the four high-impact items above before the first formal lab visit. The PCB fixes (copper keepout under FL3, stitching vias) are inexpensive at this stage and remove the main EMC unknowns. The choke and Y-cap reviews avoid a late safety surprise. The full report extends each finding with traceability to standard clauses and a recommended test plan.

02 · Scope and method

Scope and method

This document is a preliminary engineering review based only on publicly available project information for the OwnTech Foundation micro-inverter (github.com/owntech-foundation/micro-inverter). It is not a certification report, declaration of conformity, CE marking assessment, or substitute for accredited laboratory testing. Its purpose is to show how EMC and safety risks can be identified early, while changes are still cheap, and before formal compliance testing.

Inputs reviewed (preview)

- Public micro-inverter schematics (KiCad sources)
- Public micro-inverter PCB layout (KiCad sources)
- OwnTech project documentation and bill of materials
- Public datasheets for the common-mode choke FL3, isolators U801/U802 and DC/DC converters U703/U704
- Reference standards: IEC 62109-1/-2, EN 50549, IEC 61000-6-x

Target markets (assumed)

- European Union — CE marking
- United Kingdom — UKCA
- Grid code: continental Europe (EN 50549-1)

Applicable regulatory areas

- EMC — Directive 2014/30/EU (EMC) and 2014/53/EU (RED, if wireless added)
- Low-voltage electrical safety — Directive 2014/35/EU (LVD) and 2001/95/EC (General Product Safety)
- PV inverter safety — IEC 62109-1 (general) and IEC 62109-2 (grid-interactive)
- Grid connection — EN 50549-1 (LV grid connection of generators up to type B)
- EMC product standards — IEC 61000-6-3 (emissions) and 61000-6-1 (immunity), residential
- RoHS — Directive 2011/65/EU (restriction of hazardous substances)

Out of scope (preview)

- Formal laboratory testing and accredited measurements
- Mechanical enclosure design, ingress protection (IP) and thermal-stress validation
- Detailed cybersecurity assessment (RED Article 3.3)
- Grid-code variants outside continental Europe (UL 1741 SB, AS/NZS 4777.2)
- Manufacturing, supply chain and lifecycle risks

03 · Product and system description

Product and system description

Intended function: convert DC power from a photovoltaic source into AC power suitable for grid-connected or AC-load operation. The design is split into a power conversion chain, control electronics and protection functions, packaged in an outdoor residential enclosure.

Power path

PV input interface (J5–J8) → DC protection and filtering → DC/DC conversion stage → DC link / energy storage → DC/AC inverter stage → AC output / grid interface (J1, J2, J3).

Control and sensing

Measurement and sensing across the power chain feed the control electronics, which run the modulation, MPPT, grid sync and protection logic. Communication and debug interfaces are exposed for development.

Isolation and protection

Common-mode chokes and Y-capacitors on the AC port handle EMC and leakage paths. Isolators U801/U802 cross the control / power-stage boundary. Auxiliary power supply feeds the low-voltage control domain.

Operating environment

Outdoor, residential, fixed installation. Skilled-user access. Temperature range –40 °C to +60 °C. Pollution degree, overvoltage category, altitude, humidity and IP rating to be completed by the project owner.

04 · Risk register — top findings

Risk register

Six findings from this review, prioritised by severity. Severity reflects impact on certification (EMC, safety) and field reliability. Each row is detailed in the chapters that follow.

ID	Area	Finding	L	I	Severity	Owner
R-EMC-P-01	PCB	Copper pour under the common-mode choke FL3	H	H	High	HW
R-EMC-P-02	PCB	Lack of stitching vias on a 4-layer stack-up	H	H	High	HW
R-EMC-S-01	Schematic	Enable pins of DC/DC converters U703 / U704 are floating	M	M	Medium	HW
R-EMC-S-02	Schematic	Unused input pins of isolators U801 / U802 are floating	M	M	Medium	HW
R-SAF-01	Safety	Choke FL3 hi-pot only specified for 3 s vs IEC 62109 60 s	M	H	Medium-High	HW
R-SAF-02	Safety	Y-capacitors to PE may push leakage near 3.5 mA limit	M	M	Medium-High	HW

05 · EMC findings — PCB review

EMC findings — PCB review

Two PCB-layout findings drive most of the EMC risk. Both are inexpensive to fix in layout and very expensive to fix once boards are in the lab.

R-EMC-P-01 · Copper pour under the common-mode choke

High

Finding: the common-mode choke FL3 sits over a DGND copper pour. The pour creates a high-frequency capacitive path that bypasses the choke, reducing or cancelling its effectiveness against common-mode currents. Risk: high — direct impact on conducted emissions margin. Action: remove the top-layer copper under the choke (add a keepout for traces and pours under the footprint). This reduces parasitic capacitance between adjacent planes and restores the choke's filtering behaviour, increasing the chances of passing the EMC conducted-emissions test.

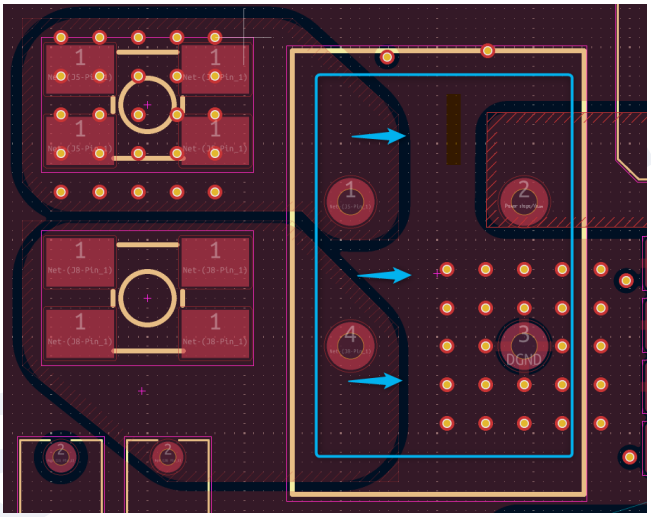

Figure: PCB top view — continuous copper pour runs directly under the common-mode choke footprint (blue arrows), instead of being cleared.

R-EMC-P-02 · Lack of stitching vias

High

Finding: the board has solid ground planes on a 4-layer stack-up — a good starting point. However, return paths are long and high impedance because there are very few stitching vias between reference planes, which causes ground bouncing and common-mode noise. Risk: high. Action: add stitching vias close to signal and power-layer transitions and along critical return-current paths. This shortens the return path, reduces loop area, limits coupling between noisy and sensitive sections, improves the high-frequency connection between reference planes and reduces both ground bounce and common-mode noise.

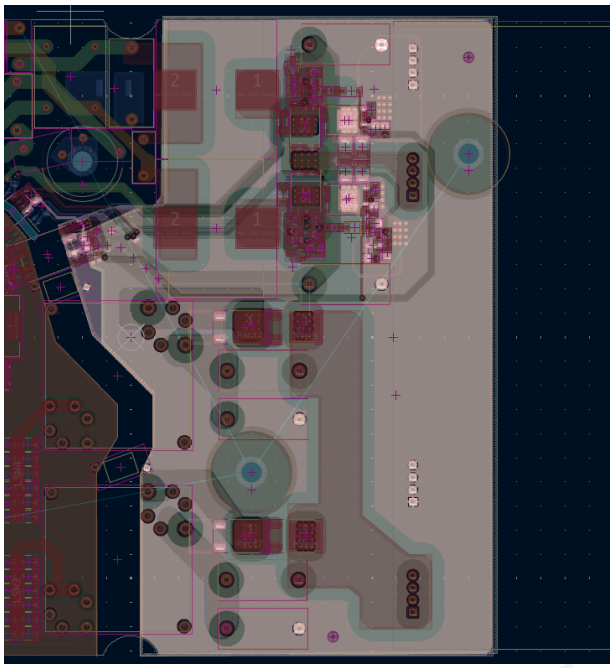

Figure: multi-layer view of the power stage — large reference-plane transitions with very few stitching vias, leaving long high-impedance return paths.

06 · EMC findings — Schematic review

EMC findings — Schematic review

Two schematic-level findings around floating pins. Both are simple to correct on the next schematic revision and remove a class of unpredictable behaviour during EMC immunity tests and in the field.

R-EMC-S-01 · Floating enable pins on DC/DC converters

Medium

Finding: the enable (EN) pins of the DC/DC converters U703 and U704 are floating. There is a microcontroller output driving them, but on power-up or under EMC immunity testing the EN state is undefined, which can lead to uncontrolled converter starts and system malfunction. Risk: medium — likely to surface during IEC 61000-4-x immunity testing. Action: add a pull-down resistor on each EN pin so the default state is well defined and the converter stays disabled until the controller drives the pin high.

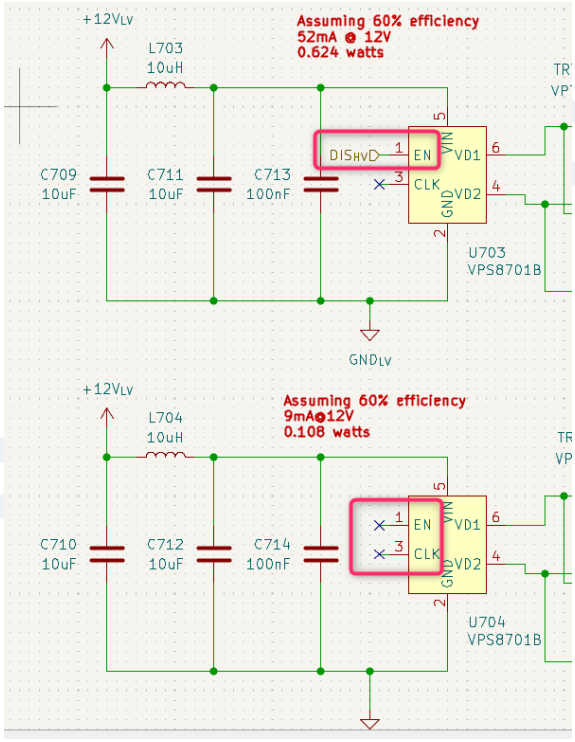

Figure: U703 EN pin driven from DIS_{HVD} with no pull-down (top); U704 EN and CLK pins left unconnected (bottom).

R-EMC-S-02 · Floating input pins on isolators

Medium

Finding: the unused input pins of the isolators U801 and U802 are left floating, so their respective output pins are unpredictable. High-frequency noise coupled into the floating inputs can cross-couple to the active channels, causing misbehaviour during normal operation or during a radiated-immunity test. Risk: medium. Action: tie the unused input pins to ground (or to a defined supply level per the isolator datasheet). The output signals stay stable, crosstalk is reduced and the immunity test margin improves.

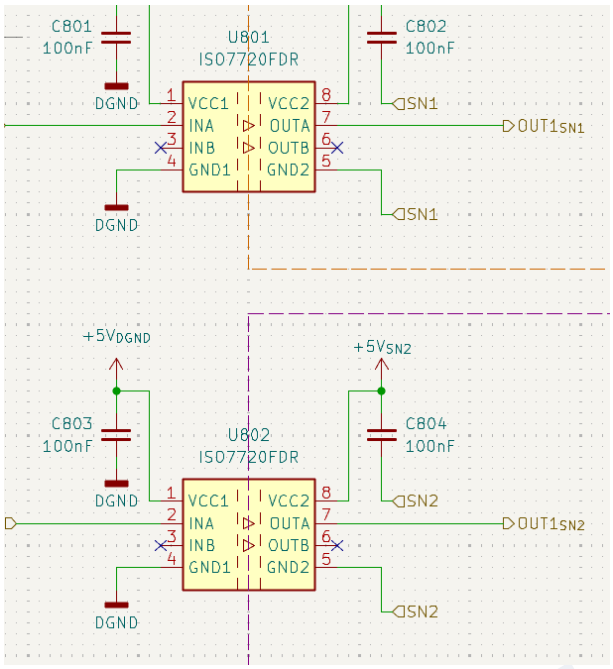

Figure: ISO7720FDR isolators U801 and U802 — INB inputs left floating while OUTB drives downstream logic.

07 · Safety risk review

Safety risk review

Two safety findings on the AC-side. Both relate to the high-pot test regime and the leakage-current budget that IEC 62109 imposes on grid-connected PV inverters.

R-SAF-01 · Common-mode choke FL3 high-pot duration

Finding: the choke FL3 (P/N PDMCAT18107-102MLB, LCSC C2997440) is specified for a high-pot test of 1.5 kV AC for only 3 seconds at 25 °C ambient. IEC 62109 demands a high-pot duration of 60 seconds, after humidity preconditioning at 92.5 %RH and 42 °C. The chosen part is therefore not directly qualified for the standard. Risk: medium-high. Recommended actions: confirm the required test voltage from the IEC 62109 isolation coordination, then either (a) test the existing choke under the standard's humidity and temperature conditions for the full 60 s, or (b) replace it with a part rated for the 60 s / humidity-conditioned regime.

R-SAF-02 · Y-capacitor leakage current

Finding: there are four 4.7 nF Y-capacitors connected to PE on the AC side. The IEC 62109 leakage-current limit for hand-held / accessible parts is 3.5 mA AC, and the combined Y-cap network — together with parasitic couplings — can push leakage close to or above that limit at nominal mains voltage. Risk: medium-high. Recommended actions: double-check the actual capacitance and the maximum allowed Y-cap value for the target leakage budget, account for parasitic couplings introduced by the layout, and re-balance the filter so leakage stays comfortably below 3.5 mA.

08 · Certification readiness and documentation

Certification readiness

Certification is achievable on the OwnTech base, provided documentation is built alongside the design rather than reconstructed afterwards. The matrix below summarises the target standards and the current readiness.

Domain	Standard	Status	Action
Safety	IEC 62109-1	At risk	Isolation-coordination table + risk file
Safety	IEC 62109-2	At risk	Fault-timing measurement + DC injection limits
Grid	EN 50549-1	At risk	Active anti-islanding + transient profile testing
EMC emissions	EN/IEC 61000-6-3	Likely pass	Pre-scan after first bring-up
EMC immunity	EN/IEC 61000-6-1	At risk	Surge/EFT coordination on AC port
Harmonics	IEC 61000-3-2	Likely pass	Confirm at lab
Documentation	Tech file + DoC	Not started	Start the structure now

If a wireless interface (Wi-Fi, BLE, LoRa) is added later, the product also falls under RED 2014/53/EU and Article 3.3 cybersecurity baseline (mandatory from 1 August 2025). Plan that scope at architecture stage rather than retrofitting.

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